What is Claimed Is:

1. An integrated circuit, comprising:

a first function block having a plurality of inputs and a plurality of outputs;

a first channel coupled to a first portion of the plurality of inputs located on a first side of the first function block and coupled to a first portion of the plurality of outputs located on the first side of the first function block;

a second channel coupled to a second portion of the plurality of inputs located on a second side of the first function block, the second side opposite the first side, and coupled to a second portion of the plurality of outputs located on the second side of the first function block;

a third channel coupled to the first channel and the second channel and coupled to a third portion of the plurality of inputs located on a third side of the first function block and coupled to a third portion of the plurality of outputs located on the third side of the first function block; and

a fourth channel associated with a fourth side of the function block that is opposite the third side, the fourth channel coupled only to the first channel and the second channel,

wherein there is at least one of: (a) a difference between any two of a number of inputs of the first, second, or third portion of the plurality of inputs, (b) a difference between any two of a number of outputs of the first, second, or third portion of the plurality of outputs, and (c) a difference between any two of the number of inputs combined with the number of outputs of the first, second, or third portion of the plurality of inputs and outputs.

2. The integrated circuit of claim 1 wherein there is a difference between any two of: (a) a number of a first plurality of wires within the first channel, (b) a number

of a second plurality of wires within the second channel, or (c) a number of a third plurality of wires within the third channel.

3. The integrated circuit of claim 1 further comprising

a wire driving device having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to a particular one of the plurality of outputs on a particular function block side that is any one of the first side, the second side, or the third side of the first function block, the wire driving device driving a signal, output by the first function block, on a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the particular function block side; and

an input multiplexer having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the first plurality of wires within the first channel, the second plurality of wires within the second channel, or the third plurality of wires within the third channel that is associated with the particular function block side,

wherein the wire driving device is upstream from the input multiplexer.

4. The integrated circuit of claim 3 wherein the wire driving device drives the signal to at least one of the particular one of the plurality of inputs of the input multiplexer, and up to a length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires minus a length of the first function block away.

5. The integrated circuit of claim 1 further comprising

an input multiplexer having a plurality of inputs and an output, the output coupled to a particular one of the plurality of inputs on a particular function block

side that is any one of the first side, the second side, or the third side of the first function block; and

a wire driving device having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to a particular one of the plurality of outputs on the particular function block side, the output of the wire driving device driving a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the particular function block side,

wherein the input multiplexer is upstream from the wire driving device.

6. The integrated circuit of claim 5 wherein the wire driving device drives a signal up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires away.

7. The integrated circuit of claim 1 further comprising

a second function block having a plurality of inputs and a plurality of outputs;

an input multiplexer having a plurality of inputs and an output, the output coupled to a particular one of the plurality of inputs of the first function block; and

a wire driving device having a plurality of inputs and an output, a first one of the plurality of inputs of the wire driving device coupled to a particular one of the plurality of outputs of the first function block, and a second one of the plurality of inputs of the wire driving device coupled to a particular one of the plurality of outputs of the second function block, and the output of the wire driving device coupled to a particular one of the plurality of inputs of the input multiplexer,

wherein the wire driving device is downstream from the second function block and the wire driving device is upstream from the input multiplexer and the first function block.

8. The integrated circuit of claim 7 wherein the output of the wire driving device is coupled to a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the wire driving device.

9. The integrated circuit of claim 8 wherein the wire driving device drives a first signal from the second function block up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires away, or the wire driving device drives a second signal from the first function block to at least one of: (a) the particular one of the plurality of inputs of the input multiplexer, and (b) up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires minus the length of the first function block away.

10. The integrated circuit of claim 1 wherein a particular one of the plurality of inputs or a particular one of the plurality of outputs of the first function block is coupled to at least two of the first channel, the second channel, or the third channel.

11. The integrated circuit of claim 10 wherein the coupling to the third channel is coupling to a particular one of a third plurality of wires within the third channel, the coupling to the first channel is coupling to a particular one of a first plurality of wires within the first channel, and the coupling to the second channel is coupling to a particular one of a second plurality of wires within the second channel.

12. The integrated circuit of claim 1 wherein a particular one of the plurality of outputs of the first function block is directly coupled to a particular one of a plurality of inputs of a second function block.

13. The integrated circuit of claim 12 wherein an input multiplexer, coupled to the second function block and having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the plurality of outputs of the first function block and the output of the input multiplexer coupled to the particular one of the plurality of inputs of the second function block.

14. The integrated circuit of claim 1 wherein the integrated circuit is a programmable logic device.

15. The integrated circuit of claim 1 wherein the first function blocks is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

16. A digital system including the integrated circuit of claim 1.

17. An integrated circuit, comprising:

a first function block having a plurality of inputs and a plurality of outputs;

a first channel coupled to a first portion of the plurality of inputs located on a first side of the first function block and coupled to a first portion of the plurality of outputs located on the first side of the first function block;

a second channel coupled to a second portion of the plurality of inputs located on a second side of the first function block, the second side opposite the first side, and coupled to a second portion of the plurality of outputs located on the second side of the first function block;

a third channel coupled to the first channel and the second channel and coupled to a third portion of the plurality of inputs located on a third side of the first function block and coupled to a third portion of the plurality of outputs located on the third side of the first function block;

a fourth channel associated with a fourth side of the function block that is opposite the third side, the fourth channel coupled only to the first channel and the second channel;

an input multiplexer having a plurality of inputs and an output, the output coupled to a particular one of the plurality of inputs on a particular function block side that is any one of the first side, the second side, or the third side of the first function block; and

a wire driving device having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to a particular one of the plurality of outputs on the particular function block side, the output of the wire driving device driving a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the particular function block side,

wherein the input multiplexer is upstream from the wire driving device.

18. The integrated circuit of claim 17 wherein the wire driving device drives a signal up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires away.

19. The integrated circuit of claim 17 wherein there is at least one of: (a) a difference between any two of a number of inputs of the first, second, or third portion of the plurality of inputs, (b) a difference between any two of a number of outputs of the first, second, or third portion of the plurality of outputs, and (c) a difference between any two of the number of inputs combined with the number of outputs of the first, second, or third portion of the plurality of inputs and outputs.

20. The integrated circuit of claim 17 wherein there is a difference between any two of: (a) a number of a first plurality of wires within the first channel, (b) a number

of a second plurality of wires within the second channel, or (c) a number of a third plurality of wires within the third channel.

21. The integrated circuit of claim 17 wherein a particular one of the plurality of inputs or a particular one of the plurality of outputs of the first function block is coupled to at least two of the first channel, the second channel, or the third channel.

22. The integrated circuit of claim 21 wherein the coupling to the third channel is coupling to another one of the third plurality of wires within the third channel, the coupling to the first channel is coupling to another one of a first plurality of wires within the first channel, and the coupling to the second channel is coupling to another one of a second plurality of wires within the second channel.

23. The integrated circuit of claim 17 wherein a particular one of the plurality of outputs of the first function block is directly coupled to a particular one of a plurality of inputs of a second function block.

24. The integrated circuit of claim 23 wherein another input multiplexer, coupled to the second function block and having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the plurality of outputs of the first function block and the output of the other input multiplexer coupled to the particular one of the plurality of inputs of the second function block.

25. The integrated circuit of claim 17 wherein the integrated circuit is a programmable logic device.

26. The integrated circuit of claim 17 wherein the first function blocks is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

27. A digital system including the integrated circuit of claim 17.

28. An integrated circuit, comprising:

a first function block having a plurality of inputs and a plurality of outputs;

a first channel coupled to a first portion of the plurality of inputs located on a first side of the first function block and coupled to a first portion of the plurality of outputs located on the first side of the first function block;

a second channel coupled to a second portion of the plurality of inputs located on a second side of the first function block, the second side opposite the first side, and coupled to a second portion of the plurality of outputs located on the second side of the first function block;

a third channel coupled to the first channel and the second channel and coupled to a third portion of the plurality of inputs located on a third side of the first function block and coupled to a third portion of the plurality of outputs located on the third side of the first function block;

a fourth channel associated with a fourth side of the function block that is opposite the third side, the fourth channel coupled only to the first channel and the second channel;

a second function block having a plurality of inputs and a plurality of outputs;

an input multiplexer having a plurality of inputs and an output, the output coupled to a particular one of the plurality of inputs of the first function block; and

a wire driving device having a plurality of inputs and an output, a first one of the plurality of inputs of the wire driving device coupled to a particular one of the plurality of outputs of the first function block, and a second one of the plurality of inputs of the wire driving device coupled to a particular one of the plurality of outputs of the second function block, and the output of the wire driving device coupled to a particular one of the plurality of inputs of the input multiplexer,

wherein the wire driving device is downstream from the second function block and the wire driving device is upstream from the input multiplexer and the first function block.

29. The integrated circuit of claim 28 wherein the output of the wire driving device is coupled to a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the wire driving device.

30. The integrated circuit of claim 29 wherein the wire driving device drives a first signal from the second function block up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires away, or the wire driving device drives a second signal from the first function block to at least one of: (a) the particular one of the plurality of inputs of the input multiplexer, and (b) up to the length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires minus the length of the first function block away.

31. The integrated circuit of claim 28 wherein there is at least one of: (a) a difference between any two of a number of inputs of the first, second, or third portion of the plurality of inputs, (b) a difference between any two of a number of outputs of the first, second, or third portion of the plurality of outputs, and (c) a difference between any two of the number of inputs combined with the number of outputs of the first, second, or third portion of the plurality of inputs and outputs.

32. The integrated circuit of claim 28 wherein there is a difference between any two of: (a) a number of a first plurality of wires within the first channel, (b) a number

of a second plurality of wires within the second channel, or (c) a number of a third plurality of wires within the third channel.

33. The integrated circuit of claim 28 wherein a particular one of the plurality of inputs or a particular one of the plurality of outputs of the first function block is coupled to at least two of the first channel, the second channel, or the third channel.

34. The integrated circuit of claim 33 wherein the coupling to the third channel is coupling to a particular one of a third plurality of wires within the third channel, the coupling to the first channel is coupling to a particular one of a first plurality of wires within the first channel, and the coupling to the second channel is coupling to a particular one of a second plurality of wires within the second channel.

35. The integrated circuit of claim 28 wherein a particular one of the plurality of outputs of the first function block is directly coupled to a particular one of a plurality of inputs of a second function block.

36. The integrated circuit of claim 35 wherein another input multiplexer, coupled to the second function block and having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the plurality of outputs of the first function block and the output of the other input multiplexer coupled to the particular one of the plurality of inputs of the second function block.

37. The integrated circuit of claim 28 wherein the integrated circuit is a programmable logic device.

38. The integrated circuit of claim 28 wherein the first function blocks is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

39. A digital system including the integrated circuit of claim 28.

40. An integrated circuit, comprising:

a first function block having a plurality of inputs and a plurality of outputs;

a first channel coupled to a first portion of the plurality of inputs located on a first side of the first function block and coupled to a first portion of the plurality of outputs located on the first side of the first function block;

a second channel coupled to a second portion of the plurality of inputs located on a second side of the first function block, the second side opposite the first side, and coupled to a second portion of the plurality of outputs located on the second side of the first function block;

a third channel coupled to the first channel and the second channel and coupled to a third portion of the plurality of inputs located on a third side of the first function block and coupled to a third portion of the plurality of outputs located on the third side of the first function block;

a fourth channel located on a fourth side of the function block that is opposite the third side, the fourth channel coupled only to the first channel and the second channel;

a wire driving device having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to a particular one of the plurality of outputs on a particular function block side that is any one of the first side, the second side, or the third side of the first function block, the wire driving device driving a signal, output by the first function block, on a particular one of a first plurality of wires within the first channel, a second plurality of wires within the second channel, or a third plurality of wires within the third channel that is associated with the particular function block side; and

an input multiplexer having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the first plurality of wires within the first channel, the second plurality of wires within the second channel, or the third plurality of wires within the third channel that is associated with the particular function block side,

wherein the wire driving device is upstream from the input multiplexer.

41. The integrated circuit of claim 40 wherein the wire driving device drives the signal to at least one of the particular one of the plurality of inputs of the input multiplexer, and up to a length of the particular one of the first plurality of wires, the second plurality of wires, or the third plurality of wires minus a length of the first function block away.

42. The integrated circuit of claim 40 wherein there is at least one of: (a) a difference between any two of a number of inputs of the first, second, or third portion of the plurality of inputs, (b) a difference between any two of a number of outputs of the first, second, or third portion of the plurality of outputs, and (c) a difference between any two of the number of inputs combined with the number of outputs of the first, second, or third portion of the plurality of inputs and outputs.

43. The integrated circuit of claim 40 wherein there is a difference between any two of: (a) a number of the first plurality of wires within the first channel, (b) a number of the second plurality of wires within the second channel, or (c) a number of the third plurality of wires within the third channel.

44. The integrated circuit of claim 40 wherein a particular one of the plurality of inputs or a particular one of the plurality of outputs of the first function block is coupled to at least two of the first channel, the second channel, or the third channel.

45. The integrated circuit of claim 44 wherein the coupling to the third channel is coupling to another one of the third plurality of wires within the third channel, the coupling to the first channel is coupling to another one of the first plurality of wires within the first channel, and the coupling to the second channel is coupling to another one of the second plurality of wires within the second channel.

46. The integrated circuit of claim 38 wherein a particular one of the plurality of outputs of the first function block is directly coupled to a particular one of a plurality of inputs of a second function block.

47. The integrated circuit of claim 44 wherein another input multiplexer, coupled to the second function block and having a plurality of inputs and an output, a particular one of the plurality of inputs coupled to the particular one of the plurality of outputs of the first function block and the output of the other input multiplexer coupled to the particular one of the plurality of inputs of the second function block.

48. The integrated circuit of claim 38 wherein the integrated circuit is a programmable logic device.

49. The integrated circuit of claim 38 wherein the first function blocks is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

50. A digital system including the integrated circuit of claim 40.

51. An integrated circuit, comprising:

a function block having a plurality of inputs and a plurality of outputs;

a first channel coupled to a first portion of the plurality of inputs located on a first side of the function block and coupled to a first portion of the plurality of outputs located on the first side of the function block;

a second channel coupled to a second portion of the plurality of inputs located on a second side of the function block, the second side opposite the first side, and coupled to a second portion of the plurality of outputs located on the second side of the function block;

a third channel coupled to the first channel and the second channel and coupled to a third portion of the plurality of inputs located on a third side of the function block and coupled to a third portion of the plurality of outputs located on the third side of the function block; and

a fourth channel coupled to the first channel and the second channel and coupled to a fourth portion of the plurality of inputs located on a fourth side of the function block, the fourth side opposite the third side, and coupled to a fourth portion of the plurality of outputs located on the fourth side of the function block,

wherein there is at least one of: (a) a difference between any two of a number of inputs of the first, second, third or fourth portion of the plurality of inputs, (b) a difference between any two of a number of outputs of the first, second, third or fourth portion of the plurality of outputs, and (c) a difference between any two of the number of inputs combined with the number of outputs of the first, second, third, or fourth portion of the plurality of inputs and outputs.

52. The integrated circuit of claim 51 wherein there is at least one of: (a) a difference between the number of inputs of the third and fourth portions of the plurality of inputs, (b) a difference between the number of outputs of the third and fourth portions of the plurality of outputs, and (c) a difference between the number of inputs combined with the number of outputs of the third and fourth portions of the plurality of inputs and outputs.

53. The integrated circuit of claim 51 wherein there is a difference between any two of: (a) a number of a first plurality of wires within the first channel, (b) a number of a second plurality of wires within the second channel, (c) a number of a third plurality of wires within the third channel, or (d) a number of a fourth plurality of wires within the fourth channel.

54. The integrated circuit of claim 51 wherein the number of the third plurality of wires within the third channel differs from the number of the fourth plurality of wires within the fourth channel.

55. The integrated circuit of claim 51 wherein there is a difference between any two of: (a) a number of at least one input multiplexer and at least one wire driving device associated with the first channel, (b) a number of at least one input multiplexer and at least one wire driving device associated with the second channel, (c) a number of at least one input multiplexer and at least one wire driving device associated with the third channel, or (d) a number of at least one input multiplexer and at least one wire driving device associated with the fourth channel.

56. The integrated circuit of claim 51 wherein a number of at least one input multiplexer and at least one wire driving device associated with the third channel is different than a number of at least one input multiplexer and at least one wire driving device associated with the fourth channel.

57. The integrated circuit of claim 51 wherein the function block has a rectangular layout.

58. A method to interconnect a function block within a programmable logic array, comprising:

transmitting and receiving signals between a first portion of a plurality of pins on a first side of the function block and a first channel;

transmitting and receiving signals between a second portion of the plurality of pins on a second side of the function block and a second channel, the second side opposite the first side;

transmitting and receiving signals between a third portion of the plurality of pins on a third side of the function block and a third channel;

preventing transmission and receipt of signals between the function block and a fourth channel associated with a fourth side of the function block, the fourth side opposite the third side; and

differing any two of a number of pins of the first portion of the plurality of pins, a number of pins of the second portion of the plurality of pins, or a number of pins of the third portion of the plurality of pins.

59. The method of claim 58 further comprising

differing any two of: (a) a number of a first plurality of wires within the first channel, (b) a number of a second plurality of wires within the second channel, or (c) a number of a third plurality of wires within the third channel.

60. The method of claim 58 further comprising

at least one of: (a) driving a signal on a particular one of a plurality of wires within the first channel, the second channel, or the third channel up to a length of the particular one of the plurality of wires minus a length of the function block away, and receiving the signal on the particular one of the plurality of wires.

61. The method of claim 58 further comprising

driving a signal on a particular one of a plurality of wires within the first channel, the second channel, or the third channel up to the length of the particular one of the plurality of wires away.

62. The method of claim 58 further comprising

at least one of: (a) driving a first signal, transmitted by the function block, on a particular one of a plurality of wires within the first channel, the second channel, or the third channel up to the length of the particular one of the plurality of wires minus the length of the function block away, (b) driving a second signal, transmitted by another function block, on the particular one of the plurality of wires up to the length of the particular one of the plurality of wires away, and (c) receiving, by the function block, the first signal or the second signal on the particular one of the plurality of wires.

63. The method of claim 58 further comprising

coupling a particular one of the plurality of pins of the function block to the third channel and at least one of the first channel and the second channel.

64. The method of claim 58 further comprising directly coupling a particular one of the plurality of pins of the function block to a particular one of a plurality of pins of another function block.

65. A stubbing layout of an integrated circuit, comprising:

a first function block having a plurality of output stubs oriented in a first direction and a plurality of inputs;

a first channel oriented in a second direction, a first one of the plurality of inputs and a first one of the plurality of output stubs oriented in the first direction

coupled to at least one wire stub corresponding to at least one wire within a first channel;

a second channel oriented in the second direction, a second one of the plurality of inputs and a second one of the plurality of output stubs oriented in the first direction coupled to at least one wire stub corresponding to at least one wire within the second channel; and

a third channel oriented in the first direction, a third one of the plurality of inputs and a third one of the plurality of output stubs oriented in the first direction coupled to at least one wire within the third channel.

66. The stubbing layout of claim 65 further comprising

a first region that includes at least one input multiplexer, each of the at least one input multiplexer oriented in the second direction, and each of the at least one input multiplexer having a plurality of inputs and an output, at least one of the plurality of inputs coupled to at least one of: (a) a particular one of the plurality of output stubs oriented in the first direction of the first function block, (b) a first one of the at least one wire stub corresponding to the at least one wire within the first channel, (c) a first one of the at least one wire stub corresponding to the at least one wire within the second channel, and (d) a first one of the at least one wire within the third channel, and the output of a particular one of the at least one input multiplexer coupled to a particular one of the plurality of inputs of the first function block; and

a second region that includes at least one wire driving device, each of the at least one wire driving device oriented in the second direction, and each of the at least one wire driving device having a plurality of inputs and an output, at least one of the plurality of inputs coupled to at least one of: (a) a particular one of the plurality of output stubs oriented in the first direction of the first function block, (b) a second one of the at least one wire stub corresponding to the at least one wire within the first channel, (c) a second one of the at least one wire stub corresponding to the at least

one wire within the second channel, and (d) a second one of the at least one wire within the third channel, and the output of a particular one of the at least one wire driving device coupled to any one of a third one of the at least one wire stub corresponding to the at least one wire of the first channel, a third one of the at least one wire stub corresponding to the at least one wire of the second channel, or a third one of the at least one wire within the third channel.

67. The stubbing layout of claim 66 wherein

at least one of the plurality of inputs of the input multiplexer has an option track oriented in the second direction; and

at least one of the plurality of inputs and the output of the wire driving device has an option track oriented in the second direction,

wherein the first direction is perpendicular to the second direction.

68. The stubbing layout of claim 67 wherein at least one of

a particular one of the plurality of output stubs of the first function block is coupled to a first option track oriented in the second direction of a first one of the plurality of inputs of a particular one of the at least one wire driving device that drives toward the first function block and a second option track oriented in the second direction of the output of the particular one of the at least one wire driving device is coupled to a third option track oriented in the second direction of a first one of the plurality of inputs of a particular one of the at least one input multiplexer that corresponds to the first function block,

the particular one of the plurality of output stubs of the first function block is coupled to a fourth option track oriented in the second direction of a particular one of the plurality of inputs of a particular one of the at least one wire driving device that drives away from the first function block, and

the particular one of the plurality of output stubs of the first function block is coupled to a fifth option track oriented in the second direction of a second one of the plurality of inputs of the particular one of the at least one wire driving device that drives toward the first function block and a sixth option track oriented in the second direction of the output of the particular one of the at least one wire driving device is coupled to a seventh option track oriented in the second direction of a second one of the plurality of inputs of the particular one of the at least one input multiplexer that corresponds to the first function block, and a particular one of a plurality of output stubs of a second function block that is upstream from the first function block is coupled to an eighth option track oriented in the second direction of a third one of the plurality of inputs of the particular one of the at least one wire driving device that drives toward the first function block.

69. The stubbing layout of claim 67 wherein an option track oriented in the second direction of a particular one of the plurality of inputs of a particular one of the at least one input multiplexer that corresponds to the first function block is coupled to a particular one of a plurality of output stubs of a second function block.

70. The stubbing layout of claim 67 wherein an option track oriented in the second direction of a particular one of the plurality of inputs of a particular one of the at least one input multiplexer that corresponds to the first function block is coupled to a particular one of the plurality of output stubs of the first function block.

71. The stubbing layout of claim 65 wherein a particular one of the plurality of inputs or a particular one of the plurality of output stubs of the first function block is coupled to at least two of a particular one of the at least one wire of the third channel, a particular one of the at least one wire stub corresponding to the at least one wire of

the first channel, and a particular one of the at least one wire stub corresponding to the at least one wire of the second channel.

72. The stubbing layout of claim 65 wherein the first function blocks is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

73. A digital system including the stubbing layout of the integrated circuit of claim 65.

74. An electronic system, comprising:

a processor that includes a programmable logic device as in claim 1;

a memory to store information;

an interface; and

a bus to couple together the processor, the memory, and the interface.

75. The electronic system of claim 74 wherein the processor configures the programmable logic device.